AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A receiver comprising digital signal processing means for transmitting data corresponding to a desired frequency component from digital data in the intermediate frequency band to output the data to detection means, wherein

said digital signal processing means comprises:

a digital band-pass filter for performing digital filtering on the digital data at a first sampling rate equal to ~~an~~ first exponentiation multiple of 2 of the intermediate frequency and

an interpolation filter including a digital low pass filter for performing digital filtering on the data output from said digital band-pass filter at a second sampling rate equal to ~~an~~ second exponentiation multiple of 2 of the intermediate frequency, the second sampling rate higher than the first sampling rate, and wherein

the output data of said interpolation filter is output to said detection means.

2. (original): The receiver according to claim 1, wherein

the first sampling rate is set to four times the intermediate frequency, and

said digital band-pass filter includes an IIR filter whose multiplicand attribute is set to the value of an exponentiation multiple of 2.

3. (original): The receiver according to claim 1, wherein

the second sampling rate is set to 16 times the intermediate frequency, and

said interpolation filter includes an IIR filter whose multiplicand attribute is set to the value of an exponentiation multiple of 2.

4. (original): The receiver according to claim 1, wherein

said digital band-pass filter comprises:

a first, a second, and a third digital adders,

a first, a second, and a third digital multipliers, and

a digital delay element having a delay time twice that for the first sampling rate,

said first digital adder subtracts output data of said second digital adder from the digital data output from analog-to-digital conversion means,

said digital delay element delays output data of said first digital adder,

said first digital multiplier multiplies output data of said digital delay element by a first predetermined multiplicand attribute,

said second digital adder subtracts output data of said first digital multiplier from output data of said digital delay element,

said second digital multiplier multiplies output data of said first digital adder by a second predetermined multiplicand attribute,

said third digital multiplier multiplies output data of said digital delay element by a second predetermined multiplicand attribute, and

said third digital adder subtracts output data of said third digital multiplier from output data of said second digital multiplier and outputs the subtraction results to said interpolation filter.

5. (original): The receiver according to claim 1, wherein

said digital band-pass filter comprises:

a first filter means includes;

a first, a second, a third, and a fourth digital adders,

a first, a second, a third, and a fourth digital multipliers, and

a first and a second digital delay elements serially connected, said elements having a delay time equal to that for the first sampling rate, and

a second filter means includes;

a fifth, a sixth, a seventh, and an eighth digital adders,

a fifth, a sixth, a seventh, and an eighth digital multipliers, and

a third and a fourth digital delay elements serially connected, said elements having a delay time equal to that for the first sampling rate,

said first digital adder subtracts output data of said second digital adder from the digital data output from said analog-to-digital conversion means,

said first digital delay element delays output data of said first digital adder,

said second digital delay element delays output data of said first digital delay element,

said first digital multiplier multiplies output data of said first digital delay element by a first predetermined multiplicand attribute,

said second digital adder subtracts output data of said third digital adder from output data of said first digital multiplier,

said second digital multiplier multiplies output data of said second digital delay element by a second predetermined multiplicand attribute,

said third digital adder subtracts output data of said third digital multiplier from output data of said second digital delay element,

said third digital multiplier multiplies output data of said first digital adder by a third predetermined multiplicand attribute,

said fourth digital multiplier multiplies output data of said second digital delay element by a second predetermined multiplicand attribute,

said fourth digital adder subtracts output data of said fourth digital multiplier from output data of said third digital multiplier,

said fifth digital adder adds output data of said sixth digital adder to output data of said fourth digital multiplier,

said third digital delay element delays output data of said fifth digital adder,

said fourth digital delay element delays output data of said third digital delay element,

said fifth digital multiplier multiplies output data of said third digital delay element by a first predetermined multiplicand attribute,

said sixth digital adder subtracts output data of said fifth digital multiplier from output data of said seventh digital adder,

said sixth digital multiplier multiplies output data of said fourth digital delay element by a second predetermined multiplicand attribute,

said seventh digital adder subtracts output data of said sixth digital multiplier from output data of said fourth digital delay element,

said third digital multiplier multiplies output data of said fifth digital adder by a seventh predetermined multiplicand attribute,

said eighth digital multiplier multiplies output data of said fourth digital delay element by a second predetermined multiplicand attribute, and

said eighth digital adder subtracts output data of said eighth digital multiplier from output data of said seventh digital multiplier and outputs the subtraction results to said interpolation filter.

6. (original): The receiver according to claim 1, wherein

said interpolation filter comprises:

a low pass filter means including;

a ninth, and a tenth digital adders,

a ninth, a tenth, and an eleventh digital multipliers, and

a fifth, and a sixth digital delay elements serially connected, said elements having a delay time equal to that for the second sampling rate,

said ninth digital adder adds data supplied from said digital band-pass filter and output data of said tenth digital adder,

said fifth digital delay element delays output data of said ninth digital adder,

said sixth digital delay element delays output data of said fifth digital delay element,

said ninth digital multiplier multiplies output data of said fifth digital delay element by a ninth predetermined multiplicand attribute,

said tenth digital adder subtracts output data of said tenth digital multiplier from output data of said ninth digital multiplier,

said tenth digital multiplier multiplies output data of said sixth digital delay element by a tenth predetermined multiplicand attribute, and

said eleventh digital multiplier multiplies output data of said ninth digital delay element by an eleventh predetermined multiplicand attribute and outputs the multiplication results to said detection means.

7. (original): The receiver according to claim 1, wherein

said interpolation filter includes a plurality of said low pass filter means serially connected.

8. (original): The receiver according to claim 6, wherein

the ninth and the eleventh multiplicand attributes of said ninth and said eleventh digital multiplier are set to 2^{-2}, and

the tenth multiplicand attribute of said tenth digital multiplier are set to 2^{-1}.

9. (currently amended): A receiver comprising digital signal processing section for transmitting data corresponding to a desired frequency component from digital data in the intermediate frequency band to output the data to detection section, wherein

said digital signal processing section comprises:

a digital band-pass filter for performing digital filtering on the digital data at a first sampling rate equal to ~~a~~ first exponentiation multiple of 2 of the intermediate frequency and

an interpolation filter including a digital low pass filter for performing digital filtering on the data output from said digital band-pass filter at a second sampling rate equal to ~~an~~ second exponentiation multiple of 2 of the intermediate frequency, the second sampling rate higher than the first sampling rate, and wherein

the output data of said interpolation filter is output to said detection section.

10. (original): The receiver according to claim 9, wherein

the first sampling rate is set to four times the intermediate frequency, and

said digital band-pass filter includes an IIR filter whose multiplicand attribute is set to the value of an exponentiation multiple of 2.

11. (original): The receiver according to claim 9, wherein

the second sampling rate is set to 16 times the intermediate frequency, and

said interpolation filter includes an IIR filter whose multiplicand attribute is set to the value of an exponentiation multiple of 2.

12. (original): The receiver according to claim 9, wherein

said digital band-pass filter comprises:

a first, a second, and a third digital adders,

a first, a second, and a third digital multipliers, and

a digital delay element having a delay time twice that for the first sampling rate,

said first digital adder subtracts output data of said second digital adder from the digital data output from analog-to-digital conversion section,

said digital delay element delays output data of said first digital adder,

said first digital multiplier multiplies output data of said digital delay element by a first predetermined multiplicand attribute,

said second digital adder subtracts output data of said first digital multiplier from output data of said digital delay element,

said second digital multiplier multiplies output data of said first digital adder by a second predetermined multiplicand attribute,

said third digital multiplier multiplies output data of said digital delay element by a second predetermined multiplicand attribute, and

said third digital adder subtracts output data of said third digital multiplier from output data of said second digital multiplier and outputs the subtraction results to said interpolation filter.

13. (original): The receiver according to claim 9, wherein

said digital band-pass filter comprises:

a first filter section includes;

a first, a second, a third, and a fourth digital adders,

a first, a second, a third, and a fourth digital multipliers, and

a first and a second digital delay elements serially connected, said elements having a delay time equal to that for the first sampling rate, and

a second filter section includes;

a fifth, a sixth, a seventh, and an eighth digital adders,

a fifth, a sixth, a seventh, and an eighth digital multipliers, and

a third and a fourth digital delay elements serially connected, said elements having a delay time equal to that for the first sampling rate,

said first digital adder subtracts output data of said second digital adder from the digital data output from said analog-to-digital conversion section,

said first digital delay element delays output data of said first digital adder,

said second digital delay element delays output data of said first digital delay element,

said first digital multiplier multiplies output data of said first digital delay element by a first predetermined multiplicand attribute,

said second digital adder subtracts output data of said third digital adder from output data of said first digital multiplier,

said second digital multiplier multiplies output data of said second digital delay element by a second predetermined multiplicand attribute,

said third digital adder subtracts output data of said third digital multiplier from output data of said second digital delay element,

said third digital multiplier multiplies output data of said first digital adder by a third predetermined multiplicand attribute,

said fourth digital multiplier multiplies output data of said second digital delay element by a second predetermined multiplicand attribute,

said fourth digital adder subtracts output data of said fourth digital multiplier from output data of said third digital multiplier,

said fifth digital adder adds output data of said sixth digital adder to output data of said fourth digital multiplier,

said third digital delay element delays output data of said fifth digital adder,

said fourth digital delay element delays output data of said third digital delay element,

said fifth digital multiplier multiplies output data of said third digital delay element by a first predetermined multiplicand attribute,

said sixth digital adder subtracts output data of said fifth digital multiplier from output data of said seventh digital adder,

said sixth digital multiplier multiplies output data of said fourth digital delay element by a second predetermined multiplicand attribute,

said seventh digital adder subtracts output data of said sixth digital multiplier from output data of said fourth digital delay element,

said third digital multiplier multiplies output data of said fifth digital adder by a seventh predetermined multiplicand attribute,

said eighth digital multiplier multiplies output data of said fourth digital delay element by a second predetermined multiplicand attribute, and

said eighth digital adder subtracts output data of said eighth digital multiplier from output data of said seventh digital multiplier and outputs the subtraction results to said interpolation filter.

14. (original): The receiver according to claim 9, wherein

said interpolation filter comprises:

a low pass filter section including;

a ninth, and a tenth digital adders,

a ninth, a tenth, and an eleventh digital multipliers, and

a fifth, and a sixth digital delay elements serially connected, said elements having a delay time equal to that for the second sampling rate,

said ninth digital adder adds data supplied from said digital band-pass filter and output data of said tenth digital adder,

said fifth digital delay element delays output data of said ninth digital adder,

said sixth digital delay element delays output data of said fifth digital delay element,

said ninth digital multiplier multiplies output data of said fifth digital delay element by a ninth predetermined multiplicand attribute,

said tenth digital adder subtracts output data of said tenth digital multiplier from output data of said ninth digital multiplier,

said tenth digital multiplier multiplies output data of said sixth digital delay element by a tenth predetermined multiplicand attribute, and

said eleventh digital multiplier multiplies output data of said ninth digital delay element by an eleventh predetermined multiplicand attribute and outputs the multiplication results to said detection section.

15. (original): The receiver according to claim 14, wherein

said interpolation filter includes a plurality of said low pass filter section serially connected.

16. (original): The receiver according to claim 14, wherein

the ninth and the eleventh multiplicand attributes of said ninth and said eleventh digital multiplier are set to 2^{-2}, and

the tenth multiplicand attribute of said tenth digital multiplier are set to 2^{-1}.

17. (new): A circuit which outputs data corresponding to a first frequency component from digital data in a frequency band and which comprises:

a first digital filter circuit that digitally filters the digital data at a first sampling rate equal to 2^x times the first frequency to produce first sampled data; and

a second digital filter circuit that digitally filters the first sampled data at a second sampling rate equal to 2^y times the first frequency to produce second sampled data,

wherein x and y are integers, and

wherein the second sampling rate higher is higher than the first sampling rate.

18. (new): The circuit according to claim 17, wherein x equals two.

19. (new): The circuit according to claim 17, wherein y equals four.

20. (new): The circuit according to claim 18, wherein y equals four.

21. (new): The circuit according to claim 17, wherein said first digital filter circuit comprises an IIR filter whose multiplicand attribute equals 2^a, wherein a is an integer.

22. (new): The circuit according to claim 17, wherein said second digital filter circuit includes an IIR filter whose multiplicand attribute equals 2^b, wherein b is an integer.

23. (new): The circuit according to claim 21, wherein said second digital filter circuit includes an IIR filter whose multiplicand attribute equals 2^b, wherein b is an integer.

24. (new): The circuit according to claim 23, wherein x equals two and y equals four.

25. (new): The circuit according to claim 17, wherein the frequency band is in an intermediate frequency band.

26. (new): The circuit according to claim 17, wherein said first digital filter circuit comprises a digital band pass filter,

wherein said second digital filter circuit comprises a digital low pass filter,

wherein said digital low pass filter constitutes at least part of an interpolation filter circuit and outputs said second sampled data to a digital detection circuit, and

wherein said digital detection circuit outputs a digital detection signal based on second sampled data.